REMARKS

The Office Action mailed December 4, 2002, has been received and reviewed. Claims 1 through 10 are currently pending in the application. Claims 1, 2, 6 and 7 stand rejected. Claims 3 through 5, and 8 through 10 are allowed. (Note-the Office Action states that claims 3-6 and 8-10 are allowed however the Office Action provides a rejection to claim 6). Applicants have not amended any claims herein, and respectfully request reconsideration of the application as presented herein.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 4,903,113 to Frankeny et al.

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Frankeny et al. (U.S. Patent No. 4,903,113, hereinafter "Frankeny"). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants respectfully traverse this rejection, as hereinafter set forth. The Office Action alleges that:

> Frankeny et al discloses . . . a semiconductor substrate having active circuit devices thereon; and an on-chip capacitor 58 including at least a portion thereof being formed in an active area of the semiconductor substrate, the on-chip capacitor being operably coupled between the active devices and the carrier substrate to provide filtering capacitance for the semiconductor device." (Office Action pp. 2-3.)

Upon a close reading of Frankeny, it is determined that Frankeny discloses a "TAB ***package*** . . . on which the semiconductor device is attached [***where***] [f]our ***capacitors*** 52, 54, 56 and 58 ***are*** shown ***mounted*** across the power 60 and ground 62 lines formed by conventional technology on flexible insulating polymer from 64 at each corner." (Col. 3, lines 3-8.) Frankeny

does not disclose an "on_chip" capacitor but rather discloses a separate and discrete "in-package" capacitor.

In contrast, Applicants claim, in part,

> 1. A semiconductor device system . . . comprising:
> a carrier substrate; and
> a semiconductor device . . . including:
> a semiconductor substrate having active circuit devices thereon; and
> an ***on-chip capacitor*** including at least a portion thereof ***being formed in an active area of the semiconductor substrate***, ... (Emphasis added.)

Applicants claim a device including a semiconductor substrate and an on-chip capacitor ***formed in*** an active area of the semiconductor substrate rather than Frankeny's discrete capacitor mounted across the power and ground lines. Frankeny does not disclose any other capacitive connection other than through the physical mounting of a discrete capacitor above the semiconductor device. Since Frankeny does not disclose forming an on-chip capacitor in an active area of the semiconductor device, Frankeny cannot anticipate Applicants' invention as claimed. Therefore, Applicants respectfully request that the rejection of claim 1 based upon the Frankeny reference be withdrawn.

Anticipation Rejection Based on U.S. Patent No. 4,656,605 to Clayton

Claim 1 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Clayton (U.S. Patent No. 4,656,605). Applicants respectfully traverse this rejection, as hereinafter set forth. The Office Action alleges that:

> Clayton discloses . . . a semiconductor substrate having active circuit devices thereon; and an on-chip capacitor 33 including at least a portion thereof being formed in an active area of the semiconductor substrate, the on-chip capacitor being operably coupled between the active devices and the carrier substrate to provide filtering capacitance for the semiconductor device." (Office Action p. 3.)

Clayton discloses that "[a]lso ***mounted on*** the substrate of module 30 are small ceramic decoupling capacitors 33-40, having a value between 0.1 and 0.22 ufd, and connected between

each of memory chips 10-18 to suppress transient voltage spikes." (Col. 2, lines 57-61; Emphasis added.) Clayton does not disclose an "on_chip" capacitor but rather "ceramic" capacitors ***"mounted on"*** the substrate.

In contrast, Applicants claim, in part,

> 1. A semiconductor device system . . . comprising:
> a carrier substrate; and
> a semiconductor device . . . including:
> a semiconductor substrate having active circuit devices thereon; and
> an ***on-chip capacitor*** including at least a portion thereof ***being formed in an active area of the semiconductor substrate***, ... (Emphasis added.)

Applicants claim a device including a semiconductor substrate and an on-chip capacitor ***formed in*** an active area of the semiconductor substrate rather than Clayton's discrete capacitor ***mounted on*** the substrate module. Clayton does not disclose any other capacitive connection other than through the ***physical mounting of a discrete capacitor to the module***. Since Clayton does not disclose forming an on-chip capacitor in an active area of the semiconductor device, Clayton cannot anticipate Applicants' invention as claimed. Therefore, Applicants respectfully request that the rejection of claim 1 based upon the Clayton reference be withdrawn.

Anticipation Rejection Based on U.S. Patent No. 4,656,605 to Clayton

Claim 2 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Clayton (U.S. Patent No. 4,656,605). Applicants respectfully traverse this rejection, as hereinafter set forth. The Office Action alleges that:

> Clayton discloses . . . a semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising, a semiconductor substrate; active circuit devices 10-18 on the semiconductor substrate; and a capacitor 33 having at least a portion thereof formed in an active area of the semiconductor substrate, the capacitor being operably coupled to the active circuit devices to provide filtering capacitance when the semiconductor device is operably connected to a carrier substrate." (Office Action, p. 3).

As stated above, Clayton discloses that "[a]lso ***mounted on*** the substrate of module 30 are small ceramic decoupling capacitors 33-40, having a value between 0.1 and 0.22 ufd, and connected between each of memory chips 10-18 to suppress transient voltage spikes." (Col. 2, lines 57-61; Emphasis added.) Clayton does not disclose a capacitor formed in an active area of the semiconductor substrate but rather "ceramic" capacitors "mounted on" the substrate.

In contrast, Applicants claim, in part,

> 2. A semiconductor device . . . comprising:
> a semiconductor substrate;
> active circuit devices on the semiconductor substrate; and
> a ***capacitor*** having at least a portion thereof ***formed in an active area of the semiconductor substrate***, ... (Emphasis added.)

Applicants claim a device including a semiconductor substrate and a capacitor ***formed in an active area of the semiconductor substrate*** rather than Clayton's discrete capacitor mounted on the substrate module. Clayton does not disclose any other capacitive connection other than through the physical mounting of a discrete capacitor to the module. Since Clayton does not disclose a capacitor formed in an active area of the semiconductor substrate, Clayton cannot anticipate Applicants' invention as claimed. Therefore, Applicants respectfully request that the rejection of claim 2 based upon the Clayton reference be withdrawn.

Anticipation Rejection Based on U.S. Patent No. 4,903,113 to Frankeny et al.

Claim 2 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Frankeny et al. (U.S. Patent No. 4,903,113). Applicants respectfully traverse this rejection, as hereinafter set forth. The Office Action alleges that:

> Frankeny et al disclose . . . a semiconductor device for operably connection to a carrier substrate, the semiconductor device comprising, a semiconductor substrate; active circuit devices 70 on the semiconductor substrate; and a capacitor 58 having at least a portion thereof formed in an active area of the semiconductor substrate, the capacitor being operably coupled to the active circuit devices to provide filtering capacitance when the semiconductor device is operably connected to a carrier substrate. (Office Action p. 4.)

As stated above, Frankeny discloses a "TAB ***package*** . . . on which the semiconductor device is attached [***where***] [f]our ***capacitors*** 52, 54, 56 and 58 ***are*** shown ***mounted*** across the power 60 and ground 62 lines formed by conventional technology on flexible insulating polymer from 64 at each corner." (Col. 3, lines 3-8.) Frankeny does not disclose a capacitor formed in an active area of a semiconductor substrate but rather a separate and discrete "in-package" capacitor.

In contrast, Applicants claim, in part,

> 2. A semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising:
> a semiconductor substrate;
> active circuit devices on the semiconductor substrate; and
> a ***capacitor*** having at least a portion thereof ***formed in an active area of the semiconductor substrate***, the capacitor being operably coupled to the active circuit devices to provide filtering capacitance for the semiconductor device when the semiconductor device is operably connected to the carrier substrate. (Emphasis added.)

Applicants claim a device including a semiconductor substrate and a capacitor ***formed in an active area of the semiconductor substrate*** rather than Frankeny's discrete capacitor ***mounted across*** the power and ground lines. Frankeny does not disclose any other capacitive connection other than through the physical mounting of a discrete capacitor above the semiconductor device. Since Frankeny does not disclose forming a capacitor in an active area of the semiconductor device, Frankeny cannot anticipate Applicants' invention as claimed. Therefore, Applicants respectfully request that the rejection of claim 2 based upon the Frankeny reference be withdrawn.

Anticipation Rejection Based on U.S. Patent No. 4,903,113 to Frankeny et al.

Claim 6 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Frankeny et al. (U.S. Patent No. 4,903,113). Applicants respectfully traverse this rejection, as hereinafter set forth. The Office Action alleges that:

> Frankeny et al disclose . . . a semiconductor die assembly for connection to external

> circuitry, the semiconductor die assembly comprising a carrier substrate configured for providing power 60 and ground 62 for at least one semiconductor die 70 operably connected thereto; and at least one semiconductor die connected to the carrier substrate and including a semiconductor substrate having active circuit elements formed on an active areas thereof; at least one capacitor 58 on the semiconductor substrate, at least a portion of the at least one capacitor being formed on the active area, the at least one capacitor operably connected to the active circuit elements to provide filtering capacitance the at least one semiconductor die. (Office Action p. 4.)

As stated above, Frankeny discloses a "TAB ***package*** . . . on which the semiconductor device is attached [***where***] [f]our ***capacitors*** 52, 54, 56 and 58 ***are*** shown ***mounted*** across the power 60 and ground 62 lines formed by conventional technology on flexible insulating polymer from 64 at each corner." (Col. 3, lines 3-8.) Frankeny does <u>not</u> disclose a capacitor formed in an active area of the semiconductor substrate but rather a separate and discrete "in-package" capacitor.

In contrast, Applicants claim, in part,

> 6. A semiconductor die assembly . . . comprising:
> a carrier substrate configured for providing power and ground for at least one semiconductor die operably connected thereto; and
> at least one semiconductor die operably connected to the carrier substrate and including:
> a semiconductor substrate having active circuit elements formed on an active area thereof; and
> ***at least one capacitor*** on the semiconductor substrate, at least a portion of the at least one capacitor ***being formed on the active area***, the at least one capacitor being operably coupled to the active circuit elements to provide filtering capacitance for the at least one semiconductor die. (Emphasis added.)

Applicants claim a semiconductor die assembly including a semiconductor substrate and a capacitor ***formed in an active area of the semiconductor substrate*** rather than Frankeny's discrete capacitor mounted across the power and ground lines. Frankeny does not disclose any other capacitive connection other than through the ***physical mounting of a discrete capacitor above*** the semiconductor device. Since Frankeny does not disclose forming a capacitor in an active area of the semiconductor substrate, Frankeny cannot anticipate Applicants' invention as

claimed. Therefore, Applicants respectfully request that the rejection of claim 6 based upon the Frankeny reference be withdrawn.

Anticipation Rejection Based on U.S. Patent No. 4,903,113 to Frankeny et al.

Claim 7 stands rejected under 35 U.S.C. § 102(e) as being anticipated by Frankeny et al. (U.S. Patent No. 4,903,113). Applicants respectfully traverse this rejection, as hereinafter set forth. The Office Action alleges that:

> Frankeny et al disclose . . . a semiconductor device for connection to a carrier substrate configured power 60 and ground 62 thereto, the semiconductor device comprising a semiconductor substrate having active circuit elements formed on an active areas thereof; at least one capacitor 58 on the semiconductor substrate, at least a portion of the at least one capacitor being formed on the active area, the at least one capacitor operably connected to the active circuit elements to provide filtering capacitance therefrom when the semiconductor device is operably connected to a carrier substrate. (Office Action p. 5.)

As stated above, Frankeny discloses a "TAB ***package*** . . . on which the semiconductor device is attached [***where***] [f]our ***capacitors*** 52, 54, 56 and 58 ***are*** shown ***mounted*** across the power 60 and ground 62 lines formed by conventional technology on flexible insulating polymer from 64 at each corner." (Col. 3, lines 3-8.) Frankeny does not disclose a capacitor formed in an active area of the semiconductor substrate but rather a separate and discrete "in-package" capacitor.

In contrast, Applicants claim, in part,

> 7. A semiconductor device for connection to a carrier substrate configured to provide power and ground thereto, the semiconductor device comprising:
> a semiconductor substrate having active circuit elements formed on an active area thereof;
> ***at least one capacitor on the semiconductor substrate***, at least a portion of the at least one capacitor ***being formed on the active area***, the at least one capacitor operably connected to the active circuit elements to provide filtering capacitance therefor when the semiconductor device is operably connected to power and ground of the carrier substrate. (Emphasis added.)

Applicants claim a semiconductor device including at least one capacitor on the semiconductor substrate which is ***formed on the active area*** rather than Frankeny's discrete capacitor mounted across the power and ground lines. Frankeny does not disclose any other capacitive connection other than through the ***physical mounting of a discrete capacitor above*** the semiconductor device. Since Frankeny does not disclose forming a capacitor in an active area of the semiconductor substrate, Frankeny cannot anticipate Applicants' invention as claimed. Therefore, Applicants respectfully request that the rejection of claim 7 based upon the Frankeny reference be withdrawn.

Allowable Subject Matter

The Office Action states that claims 3-6 and 8-10 are allowed, however, claim 6 is rejected. Therefore, Applicants have addressed the rejection of claim 6 above and believe the Examiner intended to allow claims 3-5 and 8-10.

Applicants have not amended any claims herein as the claims as previously presented are allowable in view of the cited references.

CONCLUSION

Claims 1-10 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully submitted,

Kevin K. Johanson
Registration No. 38,506
Attorney for Applicants
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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